MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2017/2018

ECE4116 – DIGITAL COMPUTER DESIGN

(All Section / Groups)

31 MAY 2018
9:00 A.M – 11:00 A.M.
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This examination paper consists of SIX (6) pages with FOUR (4) questions only..
2. Answer ALL questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Design a full adder using combinational circuit with input data bits X and Y, and one incoming carry bit, Z to produce output bits, S and C.

i) Write the truth table. [2 marks]
ii) Draw the circuit diagram. [4 marks]
iii) Write the VHDL (Very High Speed Integrated Circuit Hardware Description Language) code for the digital circuit designed in part (ii). [5 marks]

(b) Figure Q1b shows the Finite State Machine (FSM) chart of a sequential circuit with 2 inputs, X and Y, an output, Z. Output Z is equal to "1" when inputs X and Y are equal for 2 consecutive clock cycles, and "0" otherwise

(i) Draw the Algorithmic State Machine (ASM) chart for the circuit based on the FSM. [6 marks]

(ii) Write the VHDL code to implement this sequential circuit. [8 marks]

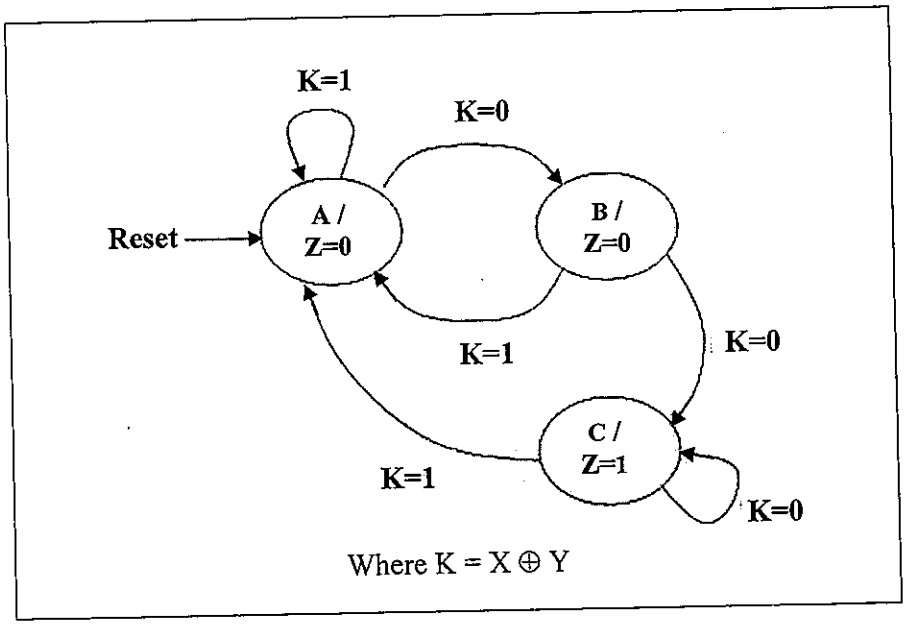

Figure Q1b

Continued...

Question 2

(a) A digital system has TWO (2) registers, R1 and R2, and control signals C_1, C_2, C_3 and C_4. The control signals control the following register transfers:

C_1: R1 ← $\overline{R2}$
C_2: R1 ← $\overline{R2}$
C_3: R1 ← R1·R2 ; logical AND
C_4: R1 ← R1+R2 ; logical OR

All the control signals are mutually-exclusive. (i.e. only one control signal can be equal to 1 at any time). No transfers occur when all control signals are equal to 0. Design the logic circuit to implement the register transfers and draw the one-bit slice logic diagram.

[10 marks]

(b) Define the 4 different types of micro-operations performed on data stored in register or memory.

[4 marks]

(c) (i) Discuss the reason why there is a need for having a memory hierarchy in any computer system.

[4 marks]

(ii) A virtual memory uses a 24-bit virtual address. Each page is 4KBytes. For a 16MByte main memory, compute the number of page frames in the main memory.

[3 marks]

(iii) Compute the number of pages in the virtual address space for the virtual memory stated in part c(ii)

[4 marks]

Continued...

Question 3

(a) Figure Q3a shows the function table of an arithmetic circuit. The inputs are 4-bit data A and B, and control signals S0 and S1. The output is a 4-bit value, F.

$S1$	$S0$	Function
0	0	$F = A$ (transfer)
0	1	$F = A + 1$ (increment)
1	0	$F = A + B$ (Addition)
1	1	$F = A + B + 1$ (Add with carry)

Figure Q3a

The arithmetic circuit consists of a parallel adder with 2 data inputs, X and Y, an output, S, carry-in, Cin, and carry-out, Cout. Data A connects to X input and data B connects to Y input. Y input might require additional logic to implement the functions given in Figure Q3a.

i) Write the truth table for X, Y, and Cin input values in terms of A, B, S0, and S1.

[4 marks]

ii) Based on the generated truth table in (i) write the Boolean expressions for X, Y and Cin inputs.

[4 marks]

iii) Y input logic is to be implemented using a 4-to-1 multiplexer. Draw the complete circuit block diagram for the arithmetic circuit.

[6 marks]

(b) An instruction is stored at location 350 with its address field at location 351. The address field has the value 2410, as shown in Figure Q3b. A processor register R1 contains the value 2310. All values are shown in decimal. Evaluate the effective address for each of the following addressing modes:

i) Direct. [2 marks]

ii) Immediate. [3 marks]

iii) Relative. [3 marks]

iv) Indexed (using register *R1* as the index register). [3 marks]

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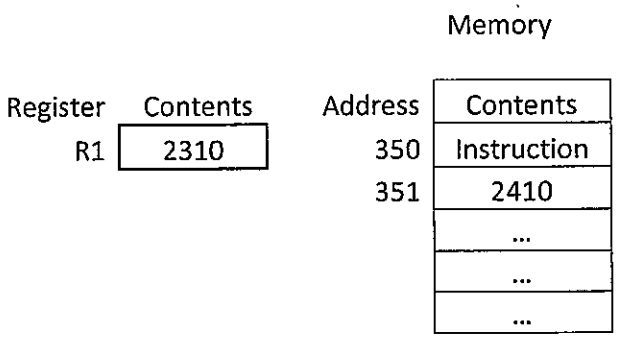

Figure Q3b

Question 4

(a) What are the two common hazards in pipelining? Explain each in detail.
[4 marks]

(b) A hypothetical Reduce Instruction Set Computer, RISC machine with the instruction format as shown in Figure Q4a and instruction specification in Figure Q4b. Given the following instruction in the Instruction Register (IR):

XRI R5 R6 1A35

i) Show the content of IR in hexadecimal value.
[4 marks]

ii) Given the content of R6 is **103B0F00**. Compute the content of R5 at the end of the instruction execution cycle.
[4 marks]

(c) A hypothetical Reduce Instruction Set Computer, RISC machine employs a typical 4-stage pipeline. You may refer to Figure Q4b for the instruction specification for this RISC machine. The following sequence of instructions is executed.

```
MOVA    R5, R7
SLT     R3, R4, R5
BZ      R3, 15
MOVA    R6, R10
```

(i) Draw the pipeline execution diagram to show the execution of the instructions. Subsequently, identify all hazards and specify what type they are.
[7 marks]

(ii) Describe the methods to resolve the hazards identified in part C(i).
[4 marks]

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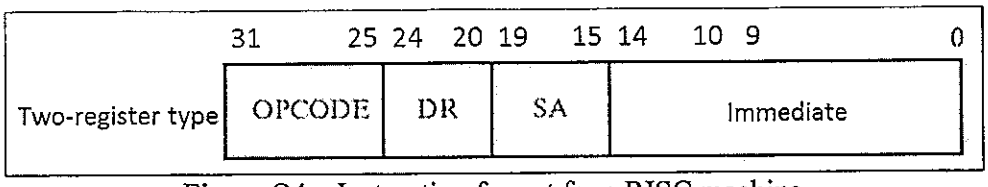

Figure Q4a: Instruction format for a RISC machine

Operation	**Symbolic Notation**	**Opcode**	**Action**
No Operation	NOP	0000000	None
Move A	MOVA	1000000	$R[DR] \leftarrow R[SA]$
Add	ADD	0000010	$R[DR] \leftarrow R[SA] + R[SB]$
Subtract	SUB	0000101	$R[DR] \leftarrow R[SA] + \overline{R[SB]} + 1$
AND	AND	0001000	$R[DR] \leftarrow R[SA] \wedge R[SB]$
OR	OR	0001001	$R[DR] \leftarrow R[SA] \vee R[SB]$
Exclusive-OR	XOR	0001010	$R[DR] \leftarrow R[SA] \oplus R[SB]$
Complement	NOT	0001011	$R[DR] \leftarrow \overline{R[SA]}$
AND Immediate	ANI	0101000	$R[DR] \leftarrow R[SA] \wedge (0 \parallel IM)$
OR Immediate	ORI	0101001	$R[DR] \leftarrow R[SA] \vee (0 \parallel IM)$
Exclusive-Or Immediate	ORI	0101010	$R[DR] \leftarrow R[SA] \oplus (0 \parallel IM)$
Add Immediate Unsigned	XRI	1000010	$R[DR] \leftarrow R[SA] + (0 \parallel IM)$
Set if Less Than	SLT	1100101	*IF* $R[SA] < R[SB]$ then $R[DR]=1$
Branch if Zero	BZ	1100000	*IF* $R[SA]=0$ *then* $PC \leftarrow PC+1+SeIM$

Figure Q4b: Instruction specification for a RISC machine

(d) Complex Instruction Set Computer, CISC machines have complex instructions, some of which require more than one execution cycle to complete. This characteristic makes it unsuitable for the standard pipelining. Describe the modification that allows the implementation of a 4-stage pipeline for a CISC machine.

[2 marks]

End of Paper